**New York Institute of Technology**

**School of Engineering and Computing Sciences**

NYIT Academy Summer Camp

VHDL Assignment 2:

Defining a Combinatorial Circuit using a Truth Table.

1. Enter the VHDL program below.

Library ieee;

Use ieee.std\_logic\_1164.all;

Entity Truth\_Table is

Port(

D : in std\_logic\_vector (1 downto 0);

Y : out std\_logic\_vector (1 downto 0));

End Truth\_Table;

Architecture Joe\_Structure of Truth\_Table is

Begin

with D select

Y <= "01" when "00",

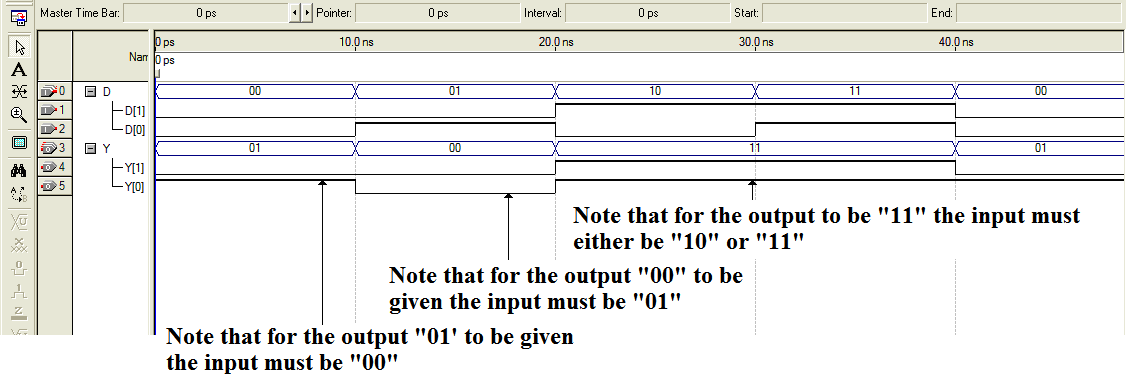
"00" when "01",

"11" when "10",

"11" when "11";

End Joe\_Structure;

1. Simulate the program and verify the truth table by using the Simulation Tool.



1. Create a VHDL truth table program for a 4 input Nand Gate.

1. Create a VHDL truth table program for a mux that has four inputs (I(0)-I(3)), one output, and two select lines. *Hint: Create a two component vector for the select lines, a four component vector for the data lines. Also, the first component of a vector I is I(0), the second component is I(1), etc.*